WHAT IS CLAIMED IS:

1. A method for receiving multiple modes of RF signals according to different radio standards having differing channel spacings, including a first channel spacing in accordance with a first standard and a second channel spacing in accordance with a second standard, wherein the first channel spacing and the second channel spacing are not directly related by integer arithmetic, comprising:

providing a reference frequency;

using the reference frequency to generate channel frequencies for the first standard;

frequency-multiplying the reference frequency by an integer number to produce a derived reference frequency; and

generating channel frequencies for the other standard using a dual-modulus synthesizer and the derived reference frequency.

2. The method of claim 1, wherein the first standard is GSM and the second standard is IS-136.

3. In a portable dual mode receiver circuit, a clock system comprising:

a baseband clock circuit;

a multiplier circuit coupled to the clock circuit for multiplying a baseband clock by a multiplier value to a master clock frequency which has as factors a first integer divider of a first channel spacing of a first band, and a second integer divider of a second channel spacing of a second band;

a programmable reference divider coupled to receive a clock signal of said master clock frequency, said programmable divider being selectively operative at said first integer divider value and at said second integer divider value to produce respectively said first channel spacing clock signal and said second channel spacing clock signal;

a digital phase detector coupled to receive output of said programmable reference divider to detect phase of said first channel spacing clock signal and said second channel spacing clock signal, said digital phase detector also having as a reference input a digital feedback signal, said digital phase detector producing as output an analog phase error signal in form of a steering voltage;

a voltage controlled oscillator (VCO) coupled to receive said phase error signal for generating a frequency controlled analog radio frequency (RF) signal at a desired frequency for system output; and

a programmable VCO divider circuit coupled to receive said analog RF signal, said programmable VCO divider circuit operative to divide frequency of said analog RF signal by a first channel integer and a second channel integer, said first and second channel integers in combination with said respective first integer divider value and said second integer divider value designate a specific channel selection in the form of said digital feedback signal.

4. The circuit according to claim 3 wherein

said baseband clock frequency is 13 MHz;

said multiplier is 3 such that said master clock frequency is 39 MHz;

said first integer divider value is 1300 for producing a channel spacing increment of 30 kHz; and wherein

said second integer divider value is 195 for producing a channel spacing increment of 200 kHz.

5. The circuit according to claim 4 wherein

said first channel integer is nominally selectable between 25,000 and 30,000; and wherein

said second channel integer is nominally selectable between 4,000 and 10,000.

6. The circuit according to claim 5 wherein

said first channel integer is nominally 28,000; and wherein

said second channel integer is nominally 4,500.

7. In a portable dual mode receiver circuit, a method for selecting channels using a clock system comprising the steps of:

generating a baseband clock signal;

multiplying said baseband clock signal by a multiplier value to a master clock frequency which has as factors a first integer divider of a first channel spacing of a first band, and a second integer divider of a second channel spacing of a second band;

programmably dividing a clock signal of said master clock frequency selectively at said first integer divider value and at said second integer divider value to

produce respectively said first channel spacing clock signal and said second channel spacing clock signal;

detecting digitally phase of said first channel spacing clock signal and said second channel spacing clock signal, with respect a reference input of a digital feedback signal, to produce as output an analog phase error signal in form of a steering voltage;

generating a frequency controlled analog radio frequency (RF) signal at a desired frequency for system output from a voltage controlled oscillator (VCO) coupled to receive said phase error signal; and

dividing frequency of said analog RF signal respectively by a first channel integer and a second channel integer in a programmable VCO divider circuit coupled to receive said analog RF signal, said first and second channel integers corresponding in combination to said respective first integer divider value and said second integer divider value to designate a specific channel selection in the form of said digital feedback signal.

8. The method according to claim 7 wherein

said baseband clock frequency is 13 MHz;

said multiplier value is 3 such that said master clock frequency is 39 MHz;

said first integer divider value is 1300 for producing a first channel spacing increment of 30 kHz; and

said second integer divider value is 195 for producing a second channel spacing increment 200 kHz.

9. The method of claim 8, wherein the first channel spacing increment corresponds to a GSM standard and the other second channel spacing increment corresponds to an IS-136 standard.